

LATCH UP TEST REPORT

Company : 南京凌鸥创芯电子有限公司

Address : 南京栖霞区兴智路 6 号兴智科技园 C 栋 1310 室

Model Name : LKS32MC081

Date Received : March 23, 2019

Date Tested : March 23, 2019

TESTING LABORATORY IS APPROVED BY:

IECQ Certificate of Approval No.: IECQ-L DEKRA 17.0004 For Independent Test Laboratory
According to ISO/IEC 17025

ISO 9001 certificate is approved by TUV CERT certification body of TUV NORD Cert GmbH

WE HEREBY CERTIFY THAT:

The test(s) shown in the attachment were conducted according to the indicating procedures. We assume full responsibility for the accuracy and completeness of these tests and vouch for the qualifications of all personnel performing them.

	Name	Signature	Date
Testing Engineer	Peng_Zhao	<i>Peng_Zhao</i>	2019/3/23
Approving Manager	Kimi Lai	<i>Kimi_Lai</i>	2019/3/23

Note :

1. This report will be invalid if reproduced in whole or in part.
2. This report refers only to the specimen(s) submitted to test, and is invalid if used separately.
3. This report is ONLY valid with the examination seal and signature of this institute.
4. The tested specimen(s) will only be preserved for thirty days from the date issued, if not collected by the applicant.



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1. GENERAL INFORMATION

1.1 DESCRIPTION OF UNIT

MANUFACTURER	: 南京凌鸥创芯电子有限公司
DEVICE NAME	: LKS32MC081
PACKAGED / PIN COUNT	: QFP48
REFERENCE DOCUMENT	: JEDEC STANDARD NO.78E NOVEMBER 2016
TRIGGER CURRENT	: 100mA (\pm); 200mA (\pm)
V SUPPLY OVER VOLTAGE TEST	: 5.5V~8.25V, Step: 1V(+);
TEST TEMPERATURE	: ROOM TEMPERATURE
PULSE DURATION	: 10 ms
SAMPLE QUANTITY	: 9 pcs
FAILURE CRITERIA	: If absolute I_{nom} is < 25 mA, then absolute $I_{nom} + 10mA$ is used; Or If absolute I_{nom} is > 25 mA, then > 1.4X absolute I_{nom} is used;

2. LATCH UP TEST

2.1 TEST EQUIPMENT

Test Equipment	Equipment S/N	Calibration Date:	Recommended Due Date:
KEYTEK ZAPMASTER MK2 768	0602221	July 10, 2018	July 9, 2019

2.2 LABORATORY AMBIENCE CONDITION

Temperature : 25±5°C

Relative humidity : 55%±10% (RH)

2.3 REFERENCE DOCUMENT

The test is based on JEDEC STANDARD NO.78E NOVEMBER 2016

2.4 TEST CONDITION

I Trigger

Over Voltage Test

2.5 SUMMARY OF TEST

Trigger Mode	Test Pin	Sample Quantity	Tested Result	V or I Limits	I Trigger : Class <u>IA</u>
I Trigger (+)	O/P1.8V	3	PASS +200mA	+2.5V	Temperature Classification: CLASS I : For Latch-up test at room temperature CLASS II : For Latch-up test at maximum-rate ambient temperature A: ≧ 100mA B: Other
	I/O5.5V		PASS +200mA	+8.25V	
I Trigger (-)	O/P1.8V	3	PASS -200mA	-0.7V	
	I/O5.5V		PASS -200mA	-2.75V	
Over Volt Test V _{supply}	VCC5.5V	3	PASS +8.25V	+600mA	

Group Set	Pin List
O/P1.8V	5
I/O5.5V	1,2,6-48
VCC5.5V	4
VSS	3

2.6 CONTENTS OF TEST

I Trigger (Positive)			
Tested Pin	Sample No. & Failed current (mA)		
	#25	#26	#27
5	PASS+200mA	PASS+200mA	PASS+200mA
1	PASS+200mA	PASS+200mA	PASS+200mA
2	PASS+200mA	PASS+200mA	PASS+200mA
6	PASS+200mA	PASS+200mA	PASS+200mA
7	PASS+200mA	PASS+200mA	PASS+200mA
8	PASS+200mA	PASS+200mA	PASS+200mA
9	PASS+200mA	PASS+200mA	PASS+200mA
10	PASS+200mA	PASS+200mA	PASS+200mA
11	PASS+200mA	PASS+200mA	PASS+200mA
12	PASS+200mA	PASS+200mA	PASS+200mA
13	PASS+200mA	PASS+200mA	PASS+200mA
14	PASS+200mA	PASS+200mA	PASS+200mA
15	PASS+200mA	PASS+200mA	PASS+200mA
16	PASS+200mA	PASS+200mA	PASS+200mA
17	PASS+200mA	PASS+200mA	PASS+200mA
18	PASS+200mA	PASS+200mA	PASS+200mA
19	PASS+200mA	PASS+200mA	PASS+200mA
20	PASS+200mA	PASS+200mA	PASS+200mA
21	PASS+200mA	PASS+200mA	PASS+200mA
22	PASS+200mA	PASS+200mA	PASS+200mA
23	PASS+200mA	PASS+200mA	PASS+200mA
24	PASS+200mA	PASS+200mA	PASS+200mA
25	PASS+200mA	PASS+200mA	PASS+200mA
26	PASS+200mA	PASS+200mA	PASS+200mA
27	PASS+200mA	PASS+200mA	PASS+200mA
28	PASS+200mA	PASS+200mA	PASS+200mA
29	PASS+200mA	PASS+200mA	PASS+200mA
30	PASS+200mA	PASS+200mA	PASS+200mA
31	PASS+200mA	PASS+200mA	PASS+200mA
32	PASS+200mA	PASS+200mA	PASS+200mA
33	PASS+200mA	PASS+200mA	PASS+200mA
34	PASS+200mA	PASS+200mA	PASS+200mA
35	PASS+200mA	PASS+200mA	PASS+200mA
36	PASS+200mA	PASS+200mA	PASS+200mA
37	PASS+200mA	PASS+200mA	PASS+200mA
38	PASS+200mA	PASS+200mA	PASS+200mA
39	PASS+200mA	PASS+200mA	PASS+200mA
40	PASS+200mA	PASS+200mA	PASS+200mA
41	PASS+200mA	PASS+200mA	PASS+200mA



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42	PASS+200mA	PASS+200mA	PASS+200mA
43	PASS+200mA	PASS+200mA	PASS+200mA
44	PASS+200mA	PASS+200mA	PASS+200mA
45	PASS+200mA	PASS+200mA	PASS+200mA
46	PASS+200mA	PASS+200mA	PASS+200mA
47	PASS+200mA	PASS+200mA	PASS+200mA
48	PASS+200mA	PASS+200mA	PASS+200mA

I Trigger (Negative)			
Tested Pin	Sample No. & Failed current (mA)		
	#28	#29	#30
5	PASS-200mA	PASS-200mA	PASS-200mA
1	PASS-200mA	PASS-200mA	PASS-200mA
2	PASS-200mA	PASS-200mA	PASS-200mA
6	PASS-200mA	PASS-200mA	PASS-200mA
7	PASS-200mA	PASS-200mA	PASS-200mA
8	PASS-200mA	PASS-200mA	PASS-200mA
9	PASS-200mA	PASS-200mA	PASS-200mA
10	PASS-200mA	PASS-200mA	PASS-200mA
11	PASS-200mA	PASS-200mA	PASS-200mA
12	PASS-200mA	PASS-200mA	PASS-200mA
13	PASS-200mA	PASS-200mA	PASS-200mA
14	PASS-200mA	PASS-200mA	PASS-200mA
15	PASS-200mA	PASS-200mA	PASS-200mA
16	PASS-200mA	PASS-200mA	PASS-200mA
17	PASS-200mA	PASS-200mA	PASS-200mA
18	PASS-200mA	PASS-200mA	PASS-200mA
19	PASS-200mA	PASS-200mA	PASS-200mA
20	PASS-200mA	PASS-200mA	PASS-200mA
21	PASS-200mA	PASS-200mA	PASS-200mA
22	PASS-200mA	PASS-200mA	PASS-200mA
23	PASS-200mA	PASS-200mA	PASS-200mA
24	PASS-200mA	PASS-200mA	PASS-200mA
25	PASS-200mA	PASS-200mA	PASS-200mA
26	PASS-200mA	PASS-200mA	PASS-200mA
27	PASS-200mA	PASS-200mA	PASS-200mA
28	PASS-200mA	PASS-200mA	PASS-200mA
29	PASS-200mA	PASS-200mA	PASS-200mA
30	PASS-200mA	PASS-200mA	PASS-200mA
31	PASS-200mA	PASS-200mA	PASS-200mA
32	PASS-200mA	PASS-200mA	PASS-200mA
33	PASS-200mA	PASS-200mA	PASS-200mA
34	PASS-200mA	PASS-200mA	PASS-200mA
35	PASS-200mA	PASS-200mA	PASS-200mA
36	PASS-200mA	PASS-200mA	PASS-200mA
37	PASS-200mA	PASS-200mA	PASS-200mA
38	PASS-200mA	PASS-200mA	PASS-200mA
39	PASS-200mA	PASS-200mA	PASS-200mA
40	PASS-200mA	PASS-200mA	PASS-200mA
41	PASS-200mA	PASS-200mA	PASS-200mA
42	PASS-200mA	PASS-200mA	PASS-200mA

43	PASS-200mA	PASS-200mA	PASS-200mA
44	PASS-200mA	PASS-200mA	PASS-200mA
45	PASS-200mA	PASS-200mA	PASS-200mA
46	PASS-200mA	PASS-200mA	PASS-200mA
47	PASS-200mA	PASS-200mA	PASS-200mA
48	PASS-200mA	PASS-200mA	PASS-200mA

Over Voltage Test for V_{supply}			
Tested Pin	Sample No. & Failed Volt (V)		
	#31	#32	#33
4	PASS+8.25V	PASS+8.25V	PASS+8.25V