Linko Semiconductor Co., Ltd.
南京凌鸥创芯电子有限公司

LKS32AT037PXL5M6Q9

32bit Compact MCU for Motor Control

Features

- 48MHz 32-bit Cortex-M0 core, hardware division coprocessor
- 30uA low-power sleep mode, MCU sleep power consumption is 30uA
- -40-125℃ Automotive-grade operating temperature range
- 2.5 V-5.5 V single power supply, internal integrated digital power supply LDO
- Super antistatic and anti-group pulse capability

Storage

- 32kB flash, with a flash anti-stealing feature
- 4kB RAM

Timer

- Built-in 4MHz high-precision RC timer, with a full temperature range accuracy of ±2%
- Built-in 64kHz low-speed timer for use in low-power mode
- Internal PLL providing up to a 48MHz timer

Peripherals

- One UART
- One SPI
- One IIC
- General-purpose 16-/32-bit timer, supporting capture and edge-aligned PWM
- Dedicated PWM module for motor control, supporting 6 PWM outputs, independent dead zone control
- Dedicated interface for Hall signals, supporting speed measurement and debounce
- 4-channel DMA
- Hardware watchdog
- Supports up to 25 GPIOs

Analog Module

- Integrated one 12-bit SAR ADC, 1Msps sampling and conversion rate, 11 channels in total
- Integrated 2 OPA, settable for a differential PGA mode
- Integrated two comparators
- Integrated 8-bit DAC digital-to-analog converter as an internal comparator input
- Built-in 1.2V voltage reference with an accuracy of 0.8%
- Built-in 1 low-power LDO and power monitoring circuit
- Integrated high-precision, low-temperature drift high-frequency RC timer

Key Strengths

✧ The internal integration of 2 high-speed operational amplifiers can meet the different requirements of single-resistor/dual-resistance current sampling topology
✧ The input port of the operational amplifier integrates a voltage clamp protection circuit, and only two external current-limiting resistors are needed to achieve direct current sampling of the MOSFET internal resistance
✧ ADC module variable gain technology can work with high-speed operational amplifiers to handle a wider dynamic range of current and take into account the sampling accuracy of small current and large current
✧ Integrated two-way comparator
✧ Strong ESD and anti-interference ability, stable and reliable
✧ Single power supply 2.5V~5.5V power supply to ensure the versatility of system power supply
✧ Supports IEC/UL60730 functional safety certification

Application Scenarios

Applicable to control systems such as BLDC/ Sensorless BLDC/ FOC/Sensorless FOC and stepping motors, permanent magnet synchronous motors, asynchronous motors, digital power source etc.

1 Overview

1.1 Function Description

LKS32AT037PXL5M6Q9 is a compact MCU with a 32-bit core for automotive electronics applications. It integrates two H-bridge circuits composed of four pairs of P-N power MOSs, which can directly drive three-phase motor windings and stepper motors..

- **Performance**
  - 48MHz 32-bit Cortex-M0 core
  - Low-power sleep mode
  - Integrated three-phase full-bridge bootstrapping gate drive modules
  - Automotive grade operating temperature range
  - Super anti-static and group pulse ability
  - AEC-Q100 Grade1 certified
- **Memory**
  - 32 kB Flash with encryption, a 128-bit chip unique identifier
  - 4kB RAM
- **Operating Range**
  - Dual power supply, MCU part adopts 2.5V ~ 5.5V power supply.
  - Operating temperature: -40~125°C
- **Timer**
  - Built-in 4MHz high-precision RC timer, with an accuracy within ±2% in a range of -40~125°C
  - Built-in 64kHz low-speed timer for use in low-power mode
  - Internal PLL providing up to a 48MHz timer
- **Peripheral Module**
  - One UART
  - One SPI for master-slave mode
  - One IIC for master-slave mode
  - One general-purpose 16-bit timer, supporting capture and edge-aligned PWM functions
  - One general-purpose 32-bit timer, supporting capture and edge-aligned PWM functions;
  - Dedicated PWM module for motor control, supporting 8 PWM outputs, independent dead zone control
  - Dedicated interface for Hall signals, supporting speed measurement and debounce functions
  - Hardware watchdog
- **Analog Module**

- Integrated one 12-bit SAR ADC, 1.2Msps sampling and conversion rate, 11 channels in total
- Integrated a 2-channel operational amplifier, settable for a differential PGA mode
- Integrated two comparators
- Integrated 8-bit DAC digital-to-analog converter
- Built-in ±2°C temperature sensor
- Built-in 1.2V voltage reference with an accuracy of 0.8%
- Built-in 1 low-power LDO and power monitoring circuit
- Integrated high-precision, low-temperature drift high-frequency RC timer

1.2 Key Strengths

- High reliability, high integration, small volume of final product, saving BOM costs.
- Internally integrated 2-channel high-speed operational amplifier and two comparators to meet the different requirements of single-resistor/dual-resistor current sampling topologies;
- Internal high-speed operational amplifier integrating high-voltage protection circuits, allowing the high-level common-mode signal to be directly input into the chip, and realizing the direct current sampling mode of MOSFET resistance with the simplest circuit topology;
- The application of patented technology enables the ADC and high-speed operational amplifier to match best, which can handle a wider current dynamic range, while taking into account the sampling accuracy of high-speed small current and low-speed large current;
- The overall control circuit is simple and efficient, with stronger anti-interference ability, more stable and reliable;
- Integrated three-phase full-bridge bootstrapping gate drive modules;
- Integrated LIN PHY
- Integrated 5V LDO

Applicable to control systems such as inductive BLDC/non-inductive BLDC/inductive FOC/non-inductive FOC and stepping motors, permanent magnet synchronous motors, asynchronous motors, etc.;

1.3 System Resources

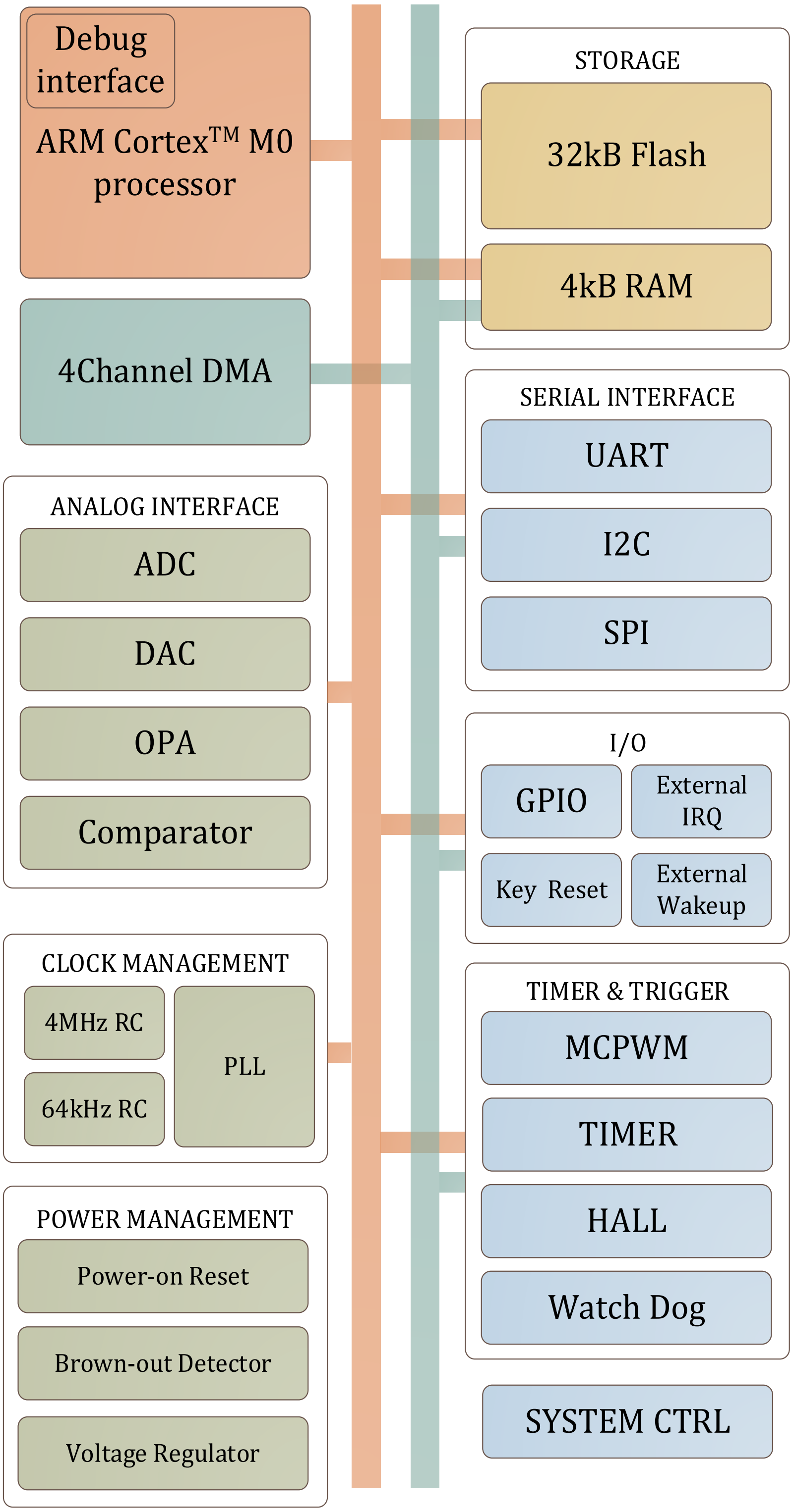

Figure 1-1 LKS32AT037PXL5M6Q9 System Block Diagram

1.4 FOC System

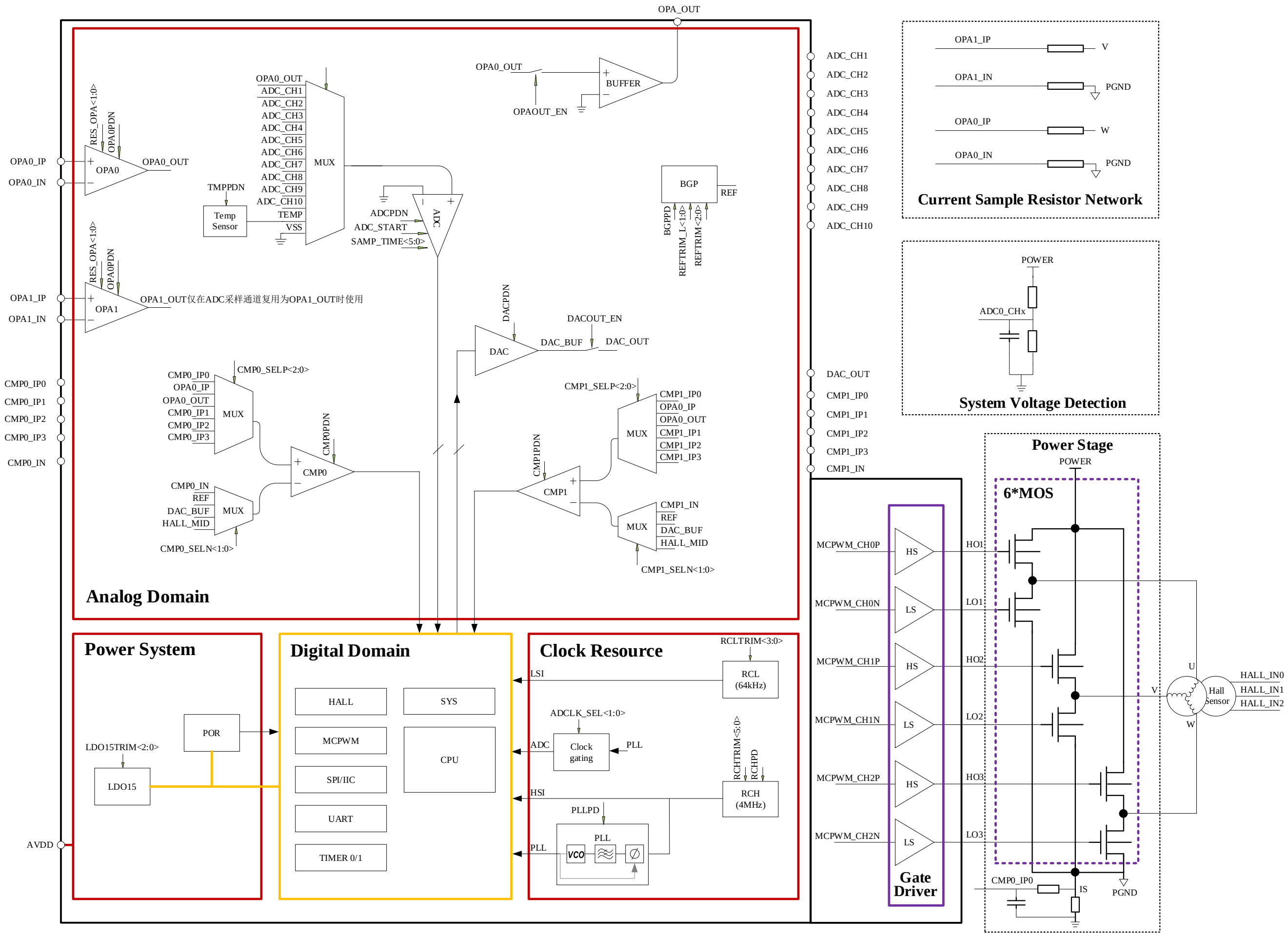

Figure 1-2 Simplified Schematic Diagram of the LKS32AT037PXL5M6Q9 Vector Sinusoidal Control System

1.5 Stepper motor control system

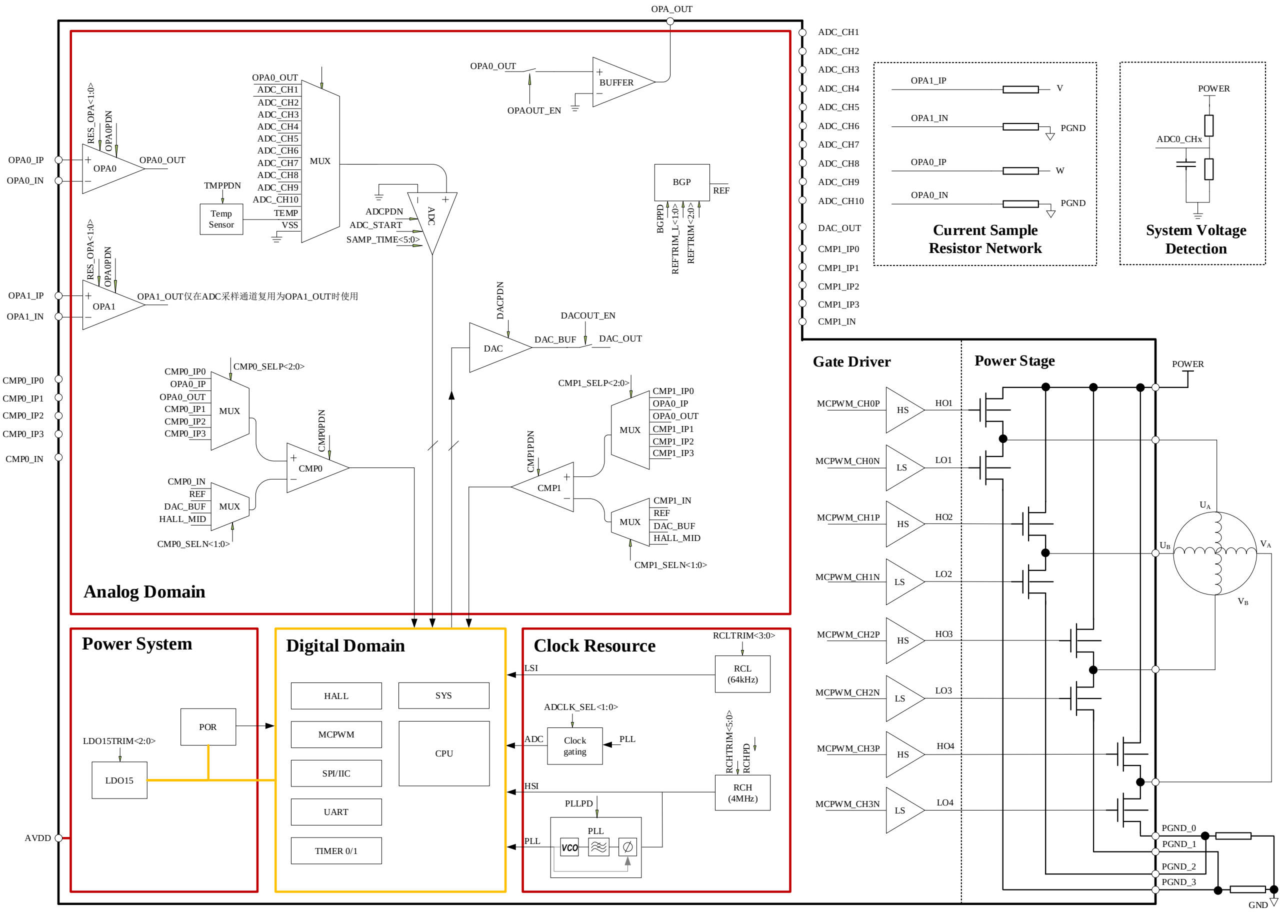

Figure 1-4 Simplified Schematic Diagram of LKS32AT037PXL5M6Q9 Stepper Motor Control System

2 Device Selection Table

Table 2-1 LKS32AT037PXL5M6Q9 Series Device Selection Table

	Frequency (MHz)	Flash (kB)	RAM (kB)	ADC ch.	DAC	Comparator	Comparator ch.	OPA	HALL	SPI	IIC	UART	CAN	Temp. Sensor	PLL	QEP	Gate driver	Gate Driver current (A)	Pre-drive supply (V)	Gate floating voltage (V)	Others	Package
LKS32AT037PXL5M6Q9*	48	32	4	10	8BITx1	2	8	2	3	1	1	1		Yes	Yes						5V LDO	QFN24

3 Pin Assignment

3.1 Pin Assignment Diagram

3.1.1 Special Notes

PU is short for pull-up. The PU pin in the following pin diagrams is designed with an internal pull-up resistor to the AVDD.

The RSTN pin is equipped with an internal 100kΩ pull-up resistor that is fixed to turn on the pull-up, which can be turned off when the RSTN function is switched to the GPIO function

The SWDIO/SWCLK has a built-in 10kΩ pull-up resistor. The pull-up is fixed on. When the SWD function is switched to the GPIO function, the pull-up can be turned off. **Since SWDIO/SWCLK is connected to the drive of the internal MOS, SWDIO/SWCLK cannot communicate when PVDD (MOS power supply) is on.**

The remaining PU pins have an internal 10kΩ pull-up resistor that can be turned on or off by software control.

EXTI is external interrupt or GPIO interrupt input pin.

WK is short for wake-up, is external wake-up source.

UARTx_TX(RX): UART supports an interchange between the TX and RX. When the second function of GPIO is selected as UART and GPIO_PIE i.e. input is enabled, it can be used as UART_RX; When GPIO_POE is enabled, it can be used as UART_TX. Generally, the same GPIO does not enable input and output at the same time, otherwise the input PDI will receive the data sent by the PDO.

SPI_DI(DO): The DI and DO of SPI can be interchanged. When the second function of GPIO is SPI, and GPIO_PIE i.e. input is enabled, it can be used as SPI_DI; when GPIO_POE i.e. output is enabled, it can be used as SPI_DO. Generally, the same GPIO does not enable input and output at the same time, otherwise the input PDI will receive the data sent by the PDO.

3.1.2 LKS32AT037PXL5M6Q9

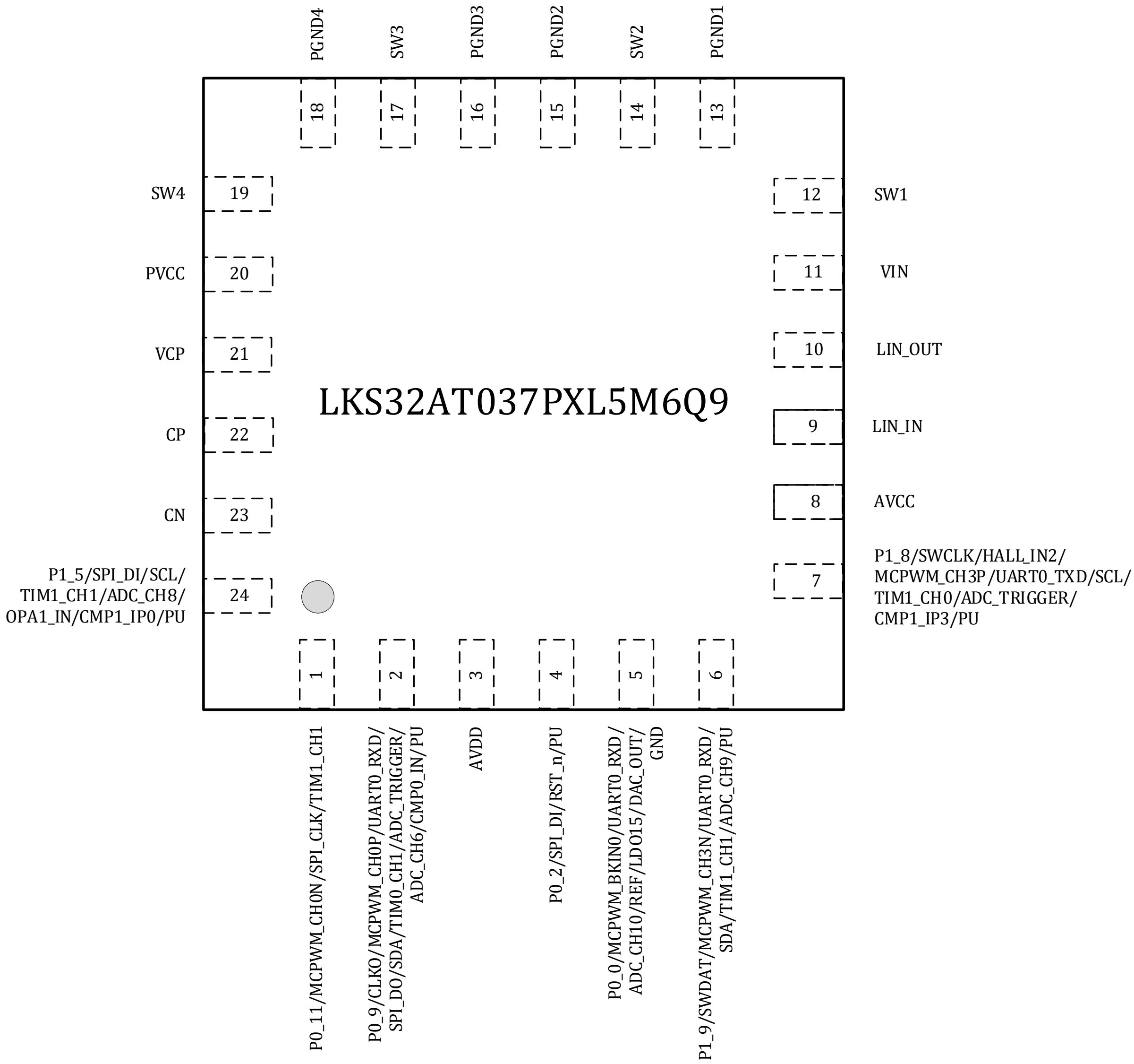

Figure 3-1 LKS32AT037PXL5M6Q9 Pin Assignment Diagram

Table 3-1 LKS32AT037PXL5M6Q9 Pin description

0	AGND	Ground
1	P0_11	P0.11
	MCPWM_CH0N	PWM channel 0 low-side
	SPI_CLK	SPI clock
	TIM1_CH1	Timer1 channel1
2	P0_9	P0.9
	CLKO	Clock output for debug

	MCPWM_CH0P	PWM channel 0 high-side
	UART0_RXD	UART0 receive(transmit)
	SPI_DO	SPI data output(input)
	SDA	I2C data
	TIM0_CH1	Timer0 channel1
	ADC_TRIGGER	ADC trigger for debug
	ADC_CH6	ADC channel 6
	CMP0_IN	Comparator0 negative input
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI7	External GPIO Interrupt Signal 7
	WK3	External wake-up signal 3
3	AVDD	Power supply, 2.2~5.5V
4	P0_2	P0.2
	SPI_DI	SPI data input(output)
	RST_n	P0.2 is used as RSTN by default. A 10nF-100nF capacitor should be connected to the ground. It is recommended a 10k-20k pull-up resistor is placed between RSTN and AVDD on PCB. If there is an external pull-up resistor, the capacitance of RSTN should be 100nF. The built-in 10kΩ pull-up resistor could be turned-off by software.
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI1	External GPIO Interrupt Signal 1
	WK1	External wake-up signal 1
5	P0_0	P0.0
	MCPWM_BKIN0	PWM break signal 0
	UART0_RXD	UART0 receive(transmit)
	ADC_CH10	ADC channel 10
	REF	Reference voltage output for debug
	LDO15	1.5V LDO output
	DAC_OUT	DAC output
	EXTI0	External GPIO Interrupt Signal 0
	WK0	External wake-up signal 0
6	P1_9	P1.9
	SWDAT	SWD Data
	MCPWM_CH3N	PWM channel 3 low-side
	UART0_RXD	UART0 receive(transmit)
	SDA	I2C data
	TIM1_CH1	Timer1 channel1
	ADC_CH9	ADC channel 9
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI15	External GPIO Interrupt Signal 15
	WK7	External wake-up signal 7
7	P1_8	P1.8
	SWCLK	SWD Clock
	HALL_IN2	Hall interface input 2

	MCPWM_CH3P	PWM channel 3 high-side
	UART0_TXD	UART0 transmit(receive)
	SCL	I2C clock
	TIM1_CH0	Timer1 channel0
	ADC_TRIGGER	ADC trigger for debug
	CMP1_IP3	Comparator1 positive input3
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI14	External GPIO Interrupt Signal 14
	WK6	External wake-up signal 6
8	AVCC	IPM Analog Power Supply Input、LIN PHY power supply
9	LIN_IN	LIN bus input, transmitting via MCU P1.6 UART0 _ TXD function, receiving and wake-up via MCU P0.8 UART0 _ TXD/WK2 function
10	LIN_OUT	LIN bus output
11	VIN	5V LDO power input.
12	SW1	The first phase output is controlled by MCPWM_CH0P of MCU P0.10. When PWM1 = 1, the upper transistor is on, the lower transistor is off, and the output SW = 1
13	PGND1	Phase 1 power ground
14	SW2	The second phase output is controlled by MCPWM _ CH1N of MCU P0.4. When PWM 1 = 1, the upper transistor is on, the lower transistor is off, and the output SW = 1
15	PGND2	Phase 2 power ground
16	PGND3	Phase 3 power ground
17	SW3	The third phase output is controlled by MCPWM _ CH2N of MCU P0.15. When PWM 1 = 1, the upper transistor is on, the lower transistor is off, and the output SW = 1.
18	PGND4	Phase 4 power ground
19	SW4	4th phase output, controlled by MCPWM _ CH3P of MCU P0.3, when PWM 1 = 1, the upper transistor is on, the lower transistor is off, and the output SW = 1
20	PVCC	MOS power supply input, it is recommended to place a 10 uF decoupling capacitor nearby to ground
21	VCP	Charge Pump Output
22	CP	Charge-pumped flying-capacitor top plate
23	CN	Charge-pumped flying-capacitor bottom plate
24	P1_5	P1.5
	SPI_DI	SPI data input(output)
	SCL	I2C clock
	TIM1_CH1	Timer1 channel1
	ADC_CH8	ADC channel 8
	OPA1_IN	OPA1 negative input
	CMP1_IP0	Comparator1 positive input0
	PU	Built-in 10kΩ Pull-up resistor which could be turn-off by software
	EXTI11	External GPIO Interrupt Signal 11
	WK5	External wake-up signal 5

Table 3-2 LKS32AT037PXL5M6Q9 Description of internal channel relationship

MCUPin definitions	Internal signal function	Description
P1_4/CMP1_OUT/MCPWM_BKIN0 /SPI_CS/TIM0_CH1/CMP1_IN/PU/EXTI1	FO	IPM fault output.When the IPM fails, pull the signal high
P1_1/OPA0_IP	CS1	Control signal of current source 1 in BSM addressing mode
P1_2/OPA0_IN	CS2	Control signal of current source 2 in BSM addressing mode
P0_0/MCPWM_BKIN0/UART0_RXD/ADC_CH10/REF/LDO15/DAC_OUT/EXTI0/WK0	VSMP1	Voltage detection channel 1
P0_5/HALL_IN1/MCPWM_BKIN1/UART0_TXD/SDA/TIM1_CH1 /ADC_CH2/CMP0_IP1/PU/EXTI3	VSMP2	Voltage detection channel 2
P0_6/HALL_IN2/ADC_CH3 /CMP0_IP0/EXTI	CSMP1	Voltage detection channel 1
P0_7/UART0_TXD/SCL/TIM0_CH1/ADC_CH5/OPAx_OUT/PU/EXTI	CSMP2	Voltage detection channel 2
P0_10/CLKO/MCPWM_CH0P/TIM0_CH0/TIM1_CH0	SW1	PWM Input for SW1
P0_4/HALL_IN0/MCPWM_CH1N/UART0_RXD/SPI_CS/SCL/TIM1_CH0/ADC_TRIGGER/ADC_CH1/CMP0_IP2/PU/EXTI2	SW2	PWM Input for SW2
P0_15/MCPWM_CH2N /TIM1_CH0/EXT9	SW3	PWM Input for SW3
P0_3/TIM1_CH0 /OPA0_IN_B	SW4	PWM Input for SW4
P1_3/SPI_CS /TIM1_CH0/OPA1_IP	SPI_CS	Chip select signal of SPI bus
1_7/CMP0_OUT/HALL_IN0/MCPWM_CH2P/UART0_RXD/TIM0_CH0/ADC_TRIGGER /CMP1_IP1/PU/EXTI13	SPI_CL	Clock signal of SPI bus
P0_13/MCPWM_CH1N /SPI_DI/TIM1_CH1	SPI_MISO	Data line of SPI bus, IPM output, MCU input
P0_12/MCPWM_CH1P /SPI_DO/TIM0_CH1	SPI_MOSI	Data line of SPI bus, MCU output, IPM input
P0_1/SPI_CS / OPA0_IP_B	SLP_N	Enable input port, high enable device enters normal mode, low disable device enters sleep mode
P0_8/CMP0_OUT/MCPWM_BKIN1/UART0_TXD/SPI_CLK/SCL/TIM0_CH0/ADC_TRIGGER /ADC_CH4/CMP0_IP3	RXD	Receiver data output (open-drain) port; held low after a wake-up event.
P1_6/CMP1_OUT/HALL_IN1/MCPWM_CH2N/UART0_TXD/TIM0_CH1/ADC_TRIGGER/ADC_CH7/CMP1_IP2	TXD	LIN Transmitter Data Input Port

3.2 Pin Multiplexing

Table 3-2 LKS32AT037PXL5M6Q9 Pin Function Selection

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF0
P0.0			MCPWM_BKIN0	UART0_R(T)XD						ADC_CH10/REF/LDO15/DAC_OUT
P0.1					MCPWM_CH3N					OPA0_IP_B
P0.2					SPI_DI(O)					RST_n
P0.3								MCPWM_CH3P		OPA0_IN_B
P0.4		HALL_IN0	MCPWM_CH1N	UART0_R(T)XD	SPI_CS	SCL		TIM1_CH0	ADC_TRIGGER	ADC_CH1/CMP0_IP2
P0.5		HALL_IN1	MCPWM_BKIN1	UART0_T(R)XD				TIM1_CH1		ADC_CH2/CMP0_IP1
P0.6		HALL_IN2								ADC_CH3/CMP0_IP0
P0.7				UART0_T(R)XD		SCL	TIM0_CH1			ADC_CH5/OPAx_OUT
P0.8	CMP0_OUT		MCPWM_BKIN1	UART0_T(R)XD	SPI_CLK	SCL	TIM0_CH0		ADC_TRIGGER	ADC_CH4/CMP0_IP3
P0.9	CLKO		MCPWM_CH0P	UART0_R(T)XD	SPI_DO(I)	SDA	TIM0_CH1		ADC_TRIGGER	ADC_CH6/CMP0_IN
P0.10	CLKO		MCPWM_CH0P				TIM0_CH0	TIM1_CH0		
P0.11			MCPWM_CH0N		SPI_CLK			TIM1_CH1		
P0.12			MCPWM_CH1P		SPI_DO(I)		TIM0_CH1			
P0.13			MCPWM_CH1N		SPI_DI(O)			TIM1_CH1		
P0.14			MCPWM_CH2P				TIM0_CH0			
P0.15			MCPWM_CH2N					TIM1_CH0		

Port	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF0
P1.1										OPA0_IP
P1.2										OPA0_IN
P1.3					SPI_CS			TIM1_CH0		OPA1_IP
P1.4	CMP1_OUT		MCPWM_BKIN0		SPI_CS		TIM0_CH1			CMP1_IN
P1.5					SPI_DI(O)	SCL		TIM1_CH1		ADC_CH8/OPA1_IN/CMP1_IP0
P1.6	CMP1_OUT	HALL_IN1	MCPWM_CH2N	UART0_T(R)XD			TIM0_CH1		ADC_TRIGGER	ADC_CH7/CMP1_IP2
P1.7	CMP0_OUT	HALL_IN0	MCPWM_CH2P	UART0_R(T)XD			SPI_CLK		ADC_TRIGGER	CMP1_IP1
P1.8	SWCLK	HALL_IN2	MCPWM_CH3P	UART0_T(R)XD		SCL		TIM1_CH0	ADC_TRIGGER	CMP1_IP3
P1.9	SWDAT		MCPWM_CH3N	UART0_R(T)XD		SDA		TIM1_CH1		ADC_CH9

4 Package Dimensions

4.1 LKS32AT037PXL5M6Q9

QFN24(4*4) Profile Quad Flat Package:

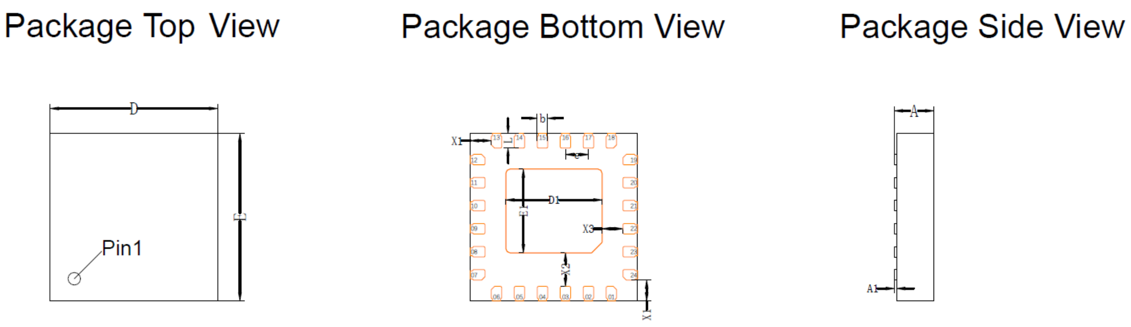

Figure 4-1 LKS32AT037PXL5M6Q9 Packaging

Table 4-2 LKS32AT037PXL5M6Q9 Packaging Dimensions

SYMBOL	MLLMETER		
	MIN	NOM	MAX
A	0.500	0.550	0.600
A1	0.007	0.012	0.017
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D1	2.250	2.300	2.350
E1	1.950	2.000	2.050
L	0.300	0.350	0.400
b	0.20	0.25	0.30
e	0.500	0.550	0.600
X1	0.450	0.500	0.550
X2	0.750	0.800	0.850
X3	0.450	0.500	0.550

5 Electrical Characteristics

The LKS32AT037PXL5M6Q9 chip is internally integrated with 8N MOS, and the electrical parameters of MCU are shown in the following table

5.1 Limit parameters

Table 5-1 LKS32AT037PXL5M6Q9 Electrical Limit Parameter

Parameter	Min	Max	Unit	Description
MCU power supply(AVDD)	-0.3	+6.0	V	
IPM Power supply voltage (PVCC)	-0.3	+40.0	V	Limiting short-time working voltage t <500ms
	-150	100	V	Limit pulse voltage, peripheral TVS and reverse diode protection
V_{LIN}	-40	40	V	Limiting pulse voltage, Reference ISO7637-2-2011
IPMAnalog Supply Voltage (AVCC)	-0.3	+40.0	V	Limiting short-time working voltage t <500ms
IPM MOSFET current	-2.0	+2.0	A	More than 800 mA requires careful heat dissipation to ensure that the die junction temperature is below 150 ˚ C
5V LDO Output current		50	mA	
Operating temperature	-40	+125	˚C	
Storage temperature	-55	+150	˚C	
Junction temperature	-	150	°C	
Pin temperature	-	300	°C	Welding, 10 seconds

If AVCC and PVCC are directly connected on the system, AVCC shall consider the same limit conditions.

Table 5-2 LKS32AT037PXL5M6Q9IO Limit parameter

Parameter	Description	Min	Max	Unit
V_{IN-LIN}	LIN pin input voltage range	-58	58	V
V_{IN}	GPIO signal input voltage range	-0.3	6.0	V
I_{INJ_PAD}	Single GPIO Maximum Injection Current	-11.2	11.2	mA
I_{INJ_SUM}	Maximum injection current of all GPIOs	-50	50	mA

5.2 Recommended operating conditions

Table 5-3 LKS32AT037PXL5M6Q9 Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit	Description
MCU Supply voltage (AVDD)	2.5	5	5.5	V	

Analog operating voltage ($AVDD_A$)	2.8	5	5.5	V	REF2VDD=0, ADC Selects 2.4V Internal Reference
	2.4	5	5.5	V	REF2VDD=1, ADC selects AVDD as reference
IPM Power supply voltage (PVCC)	8		28	V	
IPM Analog Supply Voltage (AVCC)	8		28	V	

OPA could work under 2.5V, but the output range will be limited.

5.3 ESD performance

Table 5-4 LKS32AT037PXL5M6Q9 ESD parameters

Project	Min	Max	Unit
ESD test(HBM) LIN Pin, MCU Pin	-6000	+6000	V
ESD test(HBM) other Pins	-2000	+2000	V
ESD test(CDM)	-500	+500	V

According to "MIL-STD-883J Method 3015.9", under the environment of 25°C and 55% relative humidity, electrostatic discharge is applied to all IO pins of the tested chip for 3 times, with an interval of 1s each time. The test results show that the anti-static discharge level of the chip reaches Class 3A ≧4000V, <8000V.

Table 5-5 LKS32AT037PXL5M6Q9 Latch-up parameters

Project	Min	Max	Unit
LIN/MOS output Latch-up current (25°C)	-300	+300	mA
other IO Latch-up current (25°C)	-200	+200	mA

According to "JEDEC STANDARD NO.78E NOVEMBER 2016", apply an overvoltage of 8V to all power IOs and inject 200mA of current on each signal IO. The test results show that the anti-latch-up level of the chip is 200mA.

5.4 IO characteristics

Table 5-6 LKS32AT037PXL5M6Q9 IO DC Parameter

Parameter	Description	AVDD	Condition	Min.	Max.	Unit
V_{IH}	Digital IO Input High Voltage	5V	-	0.7*AVDD		V
		3.3V		2.0		
V_{IL}	Digital IO Input Low Voltage	5V	-		0.3*AVDD	V
		3.3V			0.8	

V_{HYS}	Schmidt hysteresis range	5V 3.3V	-	0.1*AVDD		V
I_{IH}	Digital IO input high voltage, current consumption	5V 3.3V	-		1	uA
I_{IL}	Digital IO input low voltage, current consumption	5V 3.3V	-	-1		uA
V_{OH}	Digital IO Output High Voltage		Maximum drive current 11.2mA	AVDD-0.8		V
V_{OL}	Digital IO Output Low Voltage		Maximum drive current 11.2mA		0.5	V
R_{pup}	Pull-up resistor size *			8	12	kΩ
$R_{io\text{-}ana}$	Connection resistance between IO and internal analog circuit			100	200	Ω
C_{IN}	Digital IO input capacitance	5V	-		10	pF

* Only part of IOs have built-in pull-up resistors. Please refer to the pin description section for details

5.5 IPM parameters

Table 5-7 LKS32AT037PXL5M6Q9 Power MOS bridge circuit parameter

Parameter	Min.	Typ.	Max.	Unit	Description
Output current (I_{OUT_Pk})		0.8	2.0	A	VIN=16V，I_{out_Pk} = 0.81A，Tc = 125℃，At this time, the chip T_j = 145 °C; PCB double-layer board, the board thickness is 1.6mm, the copper thickness is 1 oz, and the pad size refers to the package size or demo board in Section 4; I_{OUT_Pk} = 2.0 A. The duration is mainly related to the heat dissipation of the chip, and the junction temperature of the MCU shall be kept within 150 °C. The chip can support driving BLDC motors with a phase current RMS of 1A at a maximum ring temperature of 105 degrees.
On impedance (R_{DSON})		0.5	0.8	Ω	Upper bridge + lower bridge, VCC = 12V~24V

Table 5-8 LKS32AT037PXL5M6Q9 IPM Back EMF detection

Parameter	Min.	Typ.	Max.	Unit	Description
R_{BEMF_PU}	110	140	170	kΩ	Back-EMF detection pull-up resistor

RBEMF_PD	8	10	12	kΩ	Back-EMF detection pull-down resistor
RBEMF	14.5	15	15.5	V/V	Counter electromotive force voltage division output ratio

Table 5-9 LKS32AT037PXL5M6Q9 IPM VCP Charge pump

Parameter	Min.	Typ.	Max.	Unit	Description
V_{CP}	4.9	5.2	5.5	V	Charge Pump Output Voltage, VCP-PVCC
I_{CP}	2.0			mA	Charge pump load current to meet output voltage requirement
I_{CP_LIM}	10			mA	Charge Pump Output Current Limit
V_{CP_OK}	4.45	4.6	4.85	V	VCP Undervoltage release point
V_{CP_Hyst}	4.1	4.3	4.5	V	VCP Undervoltage protection point
V_{CP_Hys}		0.3		V	VCP Undervoltage hysteresis

Table 5-10 LKS32AT037PXL5M6Q9 IPM Over-temperature protection

Parameter	Min.	Typ.	Max.	Unit	Description
T_{OTP}	140	150	160	℃	Over-temperature protection threshold， OTP = 2'b00 Gear, Refer to the user manual for specific configuration
	120	130	140	℃	Over-temperature protection threshold, OTP = 2'b01 Gear
	155	170	185	℃	Over-temperature protection threshold, OTP = 2'b10 Gear
T_{OTP_Rel}	110	120	130	℃	Over-temperature protection threshold, OTP = 2'b00 Gear
	90	100	110	℃	Over-temperature protection threshold, OTP = 2'b01 Gear
	130	140	150	℃	Over-temperature protection threshold, OTP = 2'b10 Gear

Table 5-9 LKS32AT037PXL5M6Q9 Consumption IDDQ

Clock	Operating mode	3.3V	5V	Unit
48MHz	CPU, flash, SRAM, MCPWM, Timer, and all analog modules are active, IOs stay idle	8.570	8.650	mA
4MHz	CPU, flash, SRAM, MCPWM, Timer, and all analog modules except PLL are active, IOs stay idle	3.012	3.165	mA
64kHz		2.445	2.618	mA
-	Deep Sleep Mode, PLL and BGP are turned off, only 64kHz LRC is running	27	30	uA
-	All analog modules	2.4	2.55	mA

5.6 Sleep Power Consumption

Table 5-10 LKS32AT037PXL5M6Q9 Sleep power consumption

Parameter	TEST		Min	Typical	Max	Unit
$I_{BAT}(V_{BAT})$	Quiescent mod: $V_{LIN}=V_{BAT}$ $V_{WAKE\_N}=V_{BAT}$ $V_{TXD}=0V$ $V_{SLP\_N}=0V$ $V_{BAT}=12V$		3	10	20	μA
MOS(PVDD)				280		μA
5V LDO(VIN)	Quiescent	$I_{OUT}=0mA$		3	5.5	μA
		$I_{OUT}=0.1mA$		4	6.5	μA
	Shutdown	$V_{EN}=0V$		0.4	2	μA

Unless otherwise specified, the above tests are all measured at room temperature of 25°. Due to the deviation of the device model in the manufacturing process, the current consumption of different chips will have individual differences.

5.7 Automatic addressing correlation

Table 5-12 LKS32AT037PXL5M6Q9 Automatic addressing related parameter

Parameter	Min.	Typ.	Max.	Unit	Description
t_{on_cs} Current source on time			5	us	
t_{off_cs} Current source off time			1	us	
I_{cs1}	1		1.24	mA	BSM Current in addressing mode1
I_{cs2}	3.15		3.85	mA	BSM Current in addressing mode2
Differential Error Amplifier Closed-Loop Gain	62	64	65	V/V	
R_{shunt} LIN Bus series resistance	1	1.5	2	Ω	Internal integration
I_{diff}	2.3		2.9	mA	The current threshold on R_{shunt} when the current source CS1 is closed. If it exceeds the threshold, it is considered not to be the farthest node candidate and will not participate in the next round of current measurement and identification.

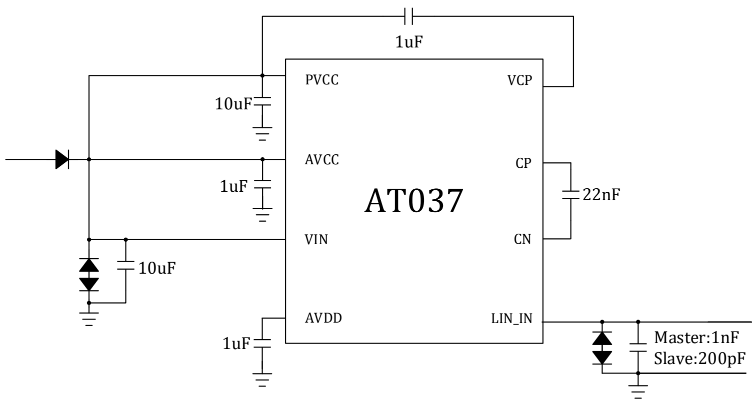

diagram 5-1 Power supply recommended application diagram

6 Analog Characteristics

Table 6-1 LKS32AT037PXL5M6Q9 Analog Characteristics

Parameter	Min.	Typ.	Max.	Unit	Description
ADC					
Supply voltage	2.8	5	5.5	V	REF2VDD=0, ADC uses internal 2.4V reference
	2.4	5	5.5	V	REF2VDD=1, ADC uses AVDD as reference
Output bitrate		1.2		MHz	$f_{adc}/20$
Differential input signal range	-2.4		+2.4	V	When Gain= 1; REF=2.4V
	-3.6		+3.6	V	When Gain=2/3; REF=3.6V
Single-ended input signal range	-0.3		AVDD+0.3	V	Limited by IO port input voltage
DC offset		5	10	mV	Correctable
Effective number of bits (ENOB)	10.5	11		bit	
INL		2	3	LSB	
DNL		1	2	LSB	
SNR	63	66		dB	
Input resistance	500k			Ohm	
Input capacitance		10p		F	
Reference voltage (REF)					
Supply voltage	2.5	5	5.5	V	
Output deviation	-9		9	mV	
Power supply rejection ratio		70		dB	
Temperature coefficient		20		ppm/°C	
Output voltage		2.4		V	
DAC					
Supply voltage	2.5	5	5.5	V	
Load resistance	50k			Ohm	
Load capacitance			50p	F	
Output voltage range	0.05		3.0	V	
Switching speed			1M	Hz	
DNL		1	2	LSB	
INL		2	4	LSB	
OFFSET		5	10	mV	
SNR	57	60	66	dB	
Operational amplifier (OPA)					

Parameter	Min.	Typ.	Max.	Unit	Description
Supply voltage	3.1	5	5.5	V	
Bandwidth		10M	20M	Hz	
Load resistance	20k			Ohm	
Load capacitance			5p	F	
Common-mode input range	0		AVDD	V	
Output signal range	0		2*Vcm	V	Minimum load resistance
OFFSET		10	15	mV	This OFFSET is the equivalent differential input deviation obtained when the OPA differential input is short-circuited and OPA OUT is measured from 0 level. The output deviation of OPA is the OPA magnification x OFFSET
Common Mode Voltage (Vcm)	1.65		2.15	V	Measurement condition: normal temperature. Operational amplifier swing=2 × min(AVDD-Vcm, Vcm). It is recommended that the application using OPA single output should be powered on to measure Vcm and make software subtraction correction. For more analysis, please refer to the official website application note "ANN009 - Differences between Operational Amplifier Differential and Single Operating Mode".
Common-mode rejection ratio (CMRR)		80		dB	
Power supply rejection ratio (PSRR)		80		dB	
Load current			500	uA	
Slew rate		5		V/us	
Phase margin		60		°	
Comparator (CMP)					
Supply voltage	2.5	5	5.5	V	
Input signal range	0		AVDD	V	
OFFSET		5	10	mV	
Transmission delay		0.15		uS	Default power consumption
		0.6		uS	Low power consumption
Hysteresis		20		mV	HYS='0'

Parameter	Min.	Typ.	Max.	Unit	Description
		0		mV	HYS='1'

Table 6-2 LKS32AT037PXL5M6Q9 5V LDO Module parameters

5V LDO					
Input Voltage	7		20	V	
Output Voltage	4.75	5	5.25	V	+/-5% Precision
Dropout Voltage		2		V	
Output Current		40		mA	
Ripple suppression		80		dB	
Input Decoupling Capacitors		0.33		uF	Added to the VCCLDO pin, see pin description section
Output Decoupling Capacitor		1		uF	Added to the VCCLDO pin, see pin description section
Operating temperature range	-40		125	°C	

Description of the analog register table:

The addresses 0x40000010-0x40000028 are the calibration registers for each module, which are provided with calibration values before being shipped from the factory. In general, you are not recommended to configure or change these values. To fine tune the analog parameters, you need to read the original calibration value.

The registers in the blank section must all be configured to 0 (reset to 0 when the chip is powered up). Other registers are configured as required by application scenarios.

7 Power Management System

7.1 Power Supply System for the AVDD Pin

The power management system consists of an LDO15 module, a power detection module (PVD), and a power-on/power-off reset module (POR).

The AVDD internally supplies power to the LDO15 module, which supplies power to all internal digital circuits and PLL modules.

The LDO15 is automatically turned on after power-up and does not require software configuration, but the LDO15 output voltage can be fine-tuned by software.

The output voltage of LDO15 can be adjusted by setting the LDO15TRIM register, as described in the analog register table. LDO 15 has been calibrated before the chip leaves the factory.

The POR module monitors the voltage of the LDO15, and provides a reset signal for the digital circuit when the voltage of the LDO15 is lower than 1.1V (for example, at the beginning of power-up or at the time of power-down), so as to prevent the digital circuit from working abnormally.

8 Clock System

The clock system consists of an internal 64kHz RC clock, an internal 4MHz RC clock, and a PLL circuit.

The 64k RC clock is used as an MCU slow clock, like the reset filter module or an MCU clock in a low power state. The 4MHz RC clock is used as the MCU main clock and, when used in conjunction with the PLL, it can provide a clock up to 48MHz.

The 64k and 4M RC clocks are factory calibrated, the 4M RC clock has a customized calibration register to further calibrate the accuracy to ±0.5%. In the temperature range of -40-105°C, the accuracy of the 64k RC clock is ±50% and that of the 4M RC clock is ±1% in this temperature range,. 4M RC clock accuracy is ±2% in -40~125℃.

The 4M RC clock is turned on by setting RCHPD = '0' (on by default, and off when set to '1'). The RC clock requires the Bandgap voltage reference module to provide reference voltage and current. Therefore, it is necessary to enable the BGP module before turning on the RC clock. The 4M RC clock is turned on and the BGP module is enabled by default in case of chip power-up. The 64k RC clock is always turned on and cannot be turned off.

The PLL multiplies the frequency of the 4M RC clock, to ensure a higher-speed clock for modules such as MCU, ADC, etc. The highest clock of the MCU and PWM modules is 48MHz, while the typical clock of the ADC module is 24MHz.

The PLL module is enabled by setting PLLPDN = '1' (off by default, and on when set to 1). The BGP (Bandgap) module needs to be enabled before the PLL module. After enabling the PLL module, it will take a stabilization time of 6us to output a stable timer. By default when the chip is powered on, the RCH timer is turned on and the BGP module is enabled; however, the PLL module is disabled, and needs to be enabled with software.

9 Reference Voltage Source

The reference voltage source provides reference voltage and current for the ADC, DAC, RC timer, PLL, temperature sensor, operational amplifier, comparator, and FLASH. The reference voltage source of BGP needs to be enabled before using any of these modules.

The BGP module is enabled by default when the chip is powered on. The reference voltage source is enabled by setting BGPPD = '0', and BGP needs about 2us to stabilize from being enabled to disabled. The output voltage of BGP is about 1.2V with an accuracy of ±0.8%

10 ADC Module

A SAR ADC is integrated into the chip. The ADC module is disabled by default when the chip is powered on. Before the ADC is enabled, it is necessary to enable the BGP and PLL modules, turn on the 4M RC timer, and select the ADC operating frequency. The ADC operating timer is 24 M by default.

The ADC requires at least 17 ADC timer cycles to complete a conversion, of which 12 are conversion cycles and 5 are sampling ones. The sampling period can be set by configuring the SAMP_TIME register in SYS_AFE_REG2. It is required to set not less than 3 sampling periods, that is, more than 8 ADC clocks.

The recommended value is 3, which corresponds to an output data rate of 1.2MHz for the ADC.

The ADC operates in the following modes: single single-channel trigger, continuous single-channel trigger, single 1-16 channel scanning, and continuous 1-16 channel scanning. Each ADC has 16 independent sets of registers for each channel.

The ADC trigger event may come from external timer signals T0, T1, T2, T3 for a preset number of times, or may be triggered by software.

The ADC has two gain modes that are set by SYS_AFE_REG0.GA_AD, corresponding to 1 x time and 2/3 x times gains. The 1 x time gain corresponds to an input signal of ±2.4V, and the 2/3 x times gain corresponds to an input signal amplitude of ±3.6V. In measuring the output signal of an operational amplifier, the specific ADC gain is selected based on the maximum possible output signal of the operational amplifier.

11 Operational Amplifier

Two input and output rail-to-rail operational amplifiers, with a built-in feedback resistor R2/R1. External pins should be connected in series with a resistor R0. The value of resistance of the feedback resistors R2:R1 can be set via register RES_OPA <1:0> for different magnification. The values corresponding to the specific registers are described in the analog register table.

The final magnification is R2/(R1+R0), where R0 is the value of resistance of the external resistor.

A capacitor greater than or equal to 15pF is required to be connected across the two input pins of the op amp.

For applications of direct sampling of MOS transistor resistor, it is recommended to connect an external resistor of >20kΩ to reduce the current flowing into the chip pins when the MOS transistor is turned off.

For small resistor sampling applications, external resistors of 100Ω are recommended.

The amplifier can select the output signal in the amplifier by setting OPAOUT_EN to send it to P0.7 IO port through BUFFER for measurement and application. Because BUFFER exists, it is also possible to send one output signal of the op amp under its normal operation mode.

In the default state when the chip is powered up, the amplifier module is turned off. The amplifier can be enabled by setting OPAPDN = '1' and the BGP module should be enabled before enabling the amplifier.

The clamping diode is built into the positive and negative input terminals of the op amp, and the motor phase line is directly connected to the input terminal through a matching resistor, thus simplifying the external circuit of MOSFET current sampling.

12 Comparator

There is a built-in 2 comparators, of which the comparison speed, the hysteresis voltage, and the signal source are programmable.

The comparator has a comparison delay of 0.15us and can also be set to less than 30ns via register CMP_FT. The hysteresis voltage is set to 20mV/0mV via CMP_HYS.

The signal source for both the positive and the negative inputs of the comparator can be programmed through the registers CMP_SELP<2:0> and CMP_SELN<1:0> as described in the register simulation instructions.

The comparator module is turned off by default when the chip is powered on. The comparator can be enabled by setting CMPx PDN =’1’ and the BGP module should be enabled before enabling the comparator.

13 Temperature Sensor

A temperature sensor with an accuracy of ±2℃ is built into the chip. The chip will undergo temperature correction before delivery, and the correction value is saved in the flash info area.

The temperature sensor module is turned off by default when the chip is powered on. The BGP module should be enabled before enabling the temperature sensor.

The temperature sensor is turned on by setting TMPPDN = '1'. It takes approximately 2us to turn on until stable, so it needs to be turned on 2us before the ADC measures the sensor.

14 DAC Module

The chip has a built-in 8bit DAC, and the range of the output signal is 1.2V/3V/4.8V.

The 8bit DAC can be configured with register DACOUT EN=1 to send the DAC output to the IO port P0.0, which can drive a load resistance >50kΩ and a load capacitor of 50pF.

The maximum output bit rate of the DAC is 1MHz.

When the chip is powered on, the DAC module is disabled by default. The DAC can be enabled by setting DACPDN =1. Before enabling the DAC module, enable the BGP module.

15 Processor

- 32-bit Cortex-M0 +DIV/SQRT coprocessor
- 2-wire SWD debugging pin
- Maximum operating frequency: 48MHz

16 Storage Resources

16.1 Flash

- The built-in flash includes a main storage area of 32kB and an information storage area of 1kB NVR
- Repeatable erasing and write-in of not less than 20,000 times
- Data is maintained for up to 100 years at a room temperature of 25℃
- The single-byte programming time is up to 7.5us, and the Sector erasing time is up to 5ms
- The Sector is 512 bytes, and can be erased or write-in by Sector. It supports runtime programming, and simultaneous erasing of and write-in to one Sector can be made while reading and accessing another Sector
- Flash data anti-theft (the last word must be written to any value other than 0xFFFFFFFF)

16.2 Execute-only Zone

Some 16kB flash capacity models are equipped with an execute-only zone of 16kB. After programming encryption, such models have the execution permission but do not have the read or write permission. Reprogramming with repeated erasure is supported.

16.3 SRAM

- Built-in 4KB SRAM

17 MCPWM Dedicated to Motor Drive

- The maximum operating timer frequency of MCPWM is 48MHz
- Supporting up to 4 channels complementary PWM outputs with adjustable phases
- The dead zone width of each channel can be configured independently
- Edge-aligned PWM mode supported
- Software control IO mode supported
- IO polarity control supported
- Internal short-circuit protection: avoiding short circuits caused by incorrect configuration
- External short-circuit protection: fast shutdown based on monitoring of external signals
- ADC sampling interrupt generates internally
- Use load register pre-memory timer to configure parameters
- The loading time and period of the loading register can be configured

* MCPWM's GPIO needs to be inserted to configure the GPIO to MOS non-conduction level before initializing to output mode

The code example is as follows:

```
GPIO0_PDO |= BIT11 | BIT13 | BIT 15 ;
GPIO0_PDO &= ~(BIT10 | BIT12 | BIT14);
…
(…GPIO Configuration…)
…
```

18 Timer

- Two general-purpose timers, one 16bit timer and one 32bit timer
- Capturing mode is supported for measuring external signal width
- Comparison mode is supported for generating edge-aligned PWM/timing interrupts

19 Hall Sensor Interface

- Built-in maximum 1024 filtering
- Three Hall signal input
- 24-bit counter with overflow and capture interrupts

20 IPM Intelligent Power Module

20.1 Drive and Power Tube

- Built-in charge pump, charge pump output voltage 5.1V, charge pump output voltage is greater than the V_{CP_OK}(4.4V) to turn on the power tube, below the V_{CP_UVLO}(4.1V) to turn off the power tube
- Built-in 4-channel N-MOS half-bridge, 4-channel PWM high-side control, upper transistor on and lower transistor off when PWM = 1, output SW = 1
- MOSFET low on-resistance 0.5Ω (sum of high-side NMOS and low-side NMOS)
- Built-in dead time 100/200/400/2000 ns (optional, 4 gears configurable)
- Built-in power tube short circuit protection, short circuit protection shielding time is T_{SCP_Blank}(0.5/1/2us, optional, 3 gears can be configured)

After the Low-side power transistor is turned on, if the VSW voltage is detected to be higher than VSW_{SCP}(2.5V) after T_{SCP_Blank} it is considered that the High-side power transistor is short-circuited. After the High-side power transistor is turned on, if the VSW voltage is detected to be lower than VSW_{SCP}(2.5V) after T_{SCP_Blank}, it is considered that the Low-side power transistor is short-circuited. Once any power transistor is detected to be short-circuited, the MCU turns off all power transistors.

20.2 5V LDO

- Load capacity greater than 50mA
- The charge pump and power transistors are turned on when the LDO output voltage is greater than the V_{LDO_OK}(4V) and turned off when the LDO output voltage is less than the V_{LDO_UVLO}(3.85V)

There is a LDO_EN enable signal inside, and the MCU can be selected to sleep without power down or sleep with power down by controlling the pull-up/pull-down of LDO_EN.

20.3 Sampling circuit

- LIN bus series resistor voltage sensing, BSM automatic addressing current sensing
- Bus voltage PVCC detection, voltage division output ratio 1/15
- Four-phase power bridge back EMF detection, divided voltage output ratio 1/15
- Four-phase current detection, two current detection gears: -0.5 ~ 0.5A/-2 ~ 2A, software optional. When -2 ~ 2A gear is selected, the voltage value obtained through the sampling

circuit is 2+I_P*0.5(V) when the current flowing into SW is +I_P; the voltage value obtained through the sampling circuit is 2+I_P*0.5(V) when the current flowing out of SW is -I_P; When -0.5 ~ 0.5A is selected, when the current flowing into SW is +I_P, the voltage value obtained by the sampling circuit is 2+I_P*2.1(V); when the current flowing out of SW is -I_P, the voltage value obtained by the sampling circuit is 2-I_P*2.1(V).

The above measured 4-channel ADC channels are subject to time division multiplexing. Refer to the User Manual interface register for the signal selection control word.

20.4 Other protection functions

- AVCC undervoltage protection. When the voltage is greater than VCC_{ON}(8.5V), the 5V LDO is turned on, and the MCU enters the normal working state. When the voltage is lower than VCC_{OFF}(7.5V), the charge pump, power tube and voltage and current sampling function are turned off (VCC_{ON}/VCC_{OFF} has another 7.5V/6.5V option).The undervoltage protection function can be cancelled, the software is optional, and the signal selection control word refers to the User Manual interface register.
- AVCC over-voltage protection, when the voltage is greater than VCC_{OV}(17.5V), the charge pump, the power tube and the voltage-current sampling function are turned off, and when the voltage is lower than the VCC_{OV_Rel}(16.5V), Charge pump, power tube and sampling function return to normal operation (VCC_{OV}/VCC_{OV_Rel} has two options of 28V/27V, 38V/37V).
- Over-temperature protection, when the temperature of the MCU is higher than T_{OTP}(150°C), the charge pump, the power tube and the voltage and current sampling function are turned off; when the temperature of the MCU is lower than the T_{OTP_Rel}(120°C), Restart the charge pump, power tube and sampling function (T_{OTP}/T_{OTP_Rel} also has two options of 130/100 °C and 170/140 °C)

21 LIN transceiver

- LIN transfers data rates up to 20kbps
- Integrated 30kΩ LIN pull-up resistor
- System-level power control using the INH pin
- Power-up/power-down glitch-free operation on LIN bus and RXD output
- Protection features: ± 58V LIN bus fault tolerance, 42V load dump support, IEC ESD protection, undervoltage protection on VBAT input, TXD dominant state timeout, thermal shutdown, system-level unpowered node or ground disconnect failure protection.
- Support LIN bus automatic addressing

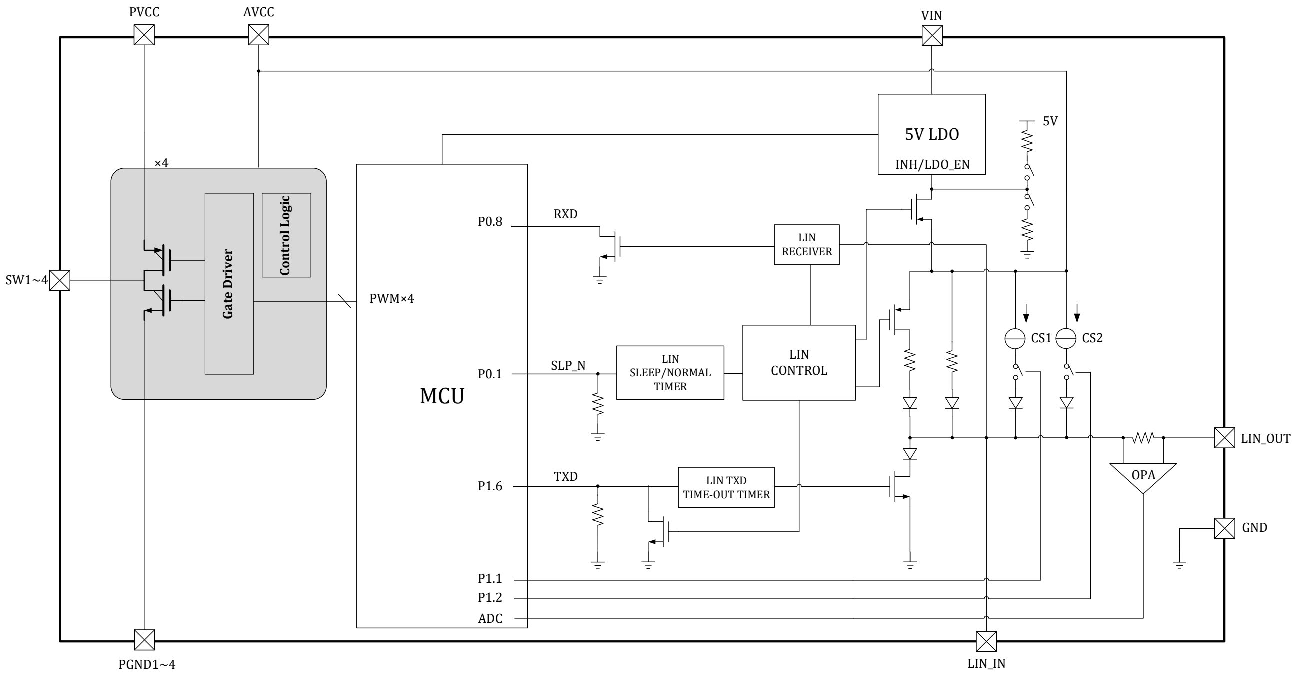

Figure 21-1 Power and sleep related pin description

The RXD pin of the LIN transceiver is connected to P0.8 of the MCU inner core, the TXD pin is connected to P1.6 of the MCU inner core, P0.1 of the MCU outer core controls the SLP_N pin of the transceiver, P1.1 and P1.2 of the MCU outer core respectively control the opening or closing of BSM automatic addressing current sources CS1 and CS2,The LIN bus series resistor differential pressure measurement is sent to the ADC sampling port of the MCU core via the built-in op amp.

In normal mode, when the MCU configuration SLP _ N signal has a falling edge and the SLP _ N is kept low for more than 10 us, the LIN-PHY enters sleep mode. The INH signal is always floating in sleep mode, and the INH pin is high in all other modes.

Depending on the application, the INH/EN pin can be externally connected with a pull-up or pull-down resistor. When the pull-down resistor is externally connected, the INH signal is pulled down by the external pull-down resistor after the LIN-PHY goes to sleep, and the 5V LDO is turned off and no longer supplies power to the MCU through AVDD. At this time, lower sleep power consumption can be obtained (VIN current of 5V LDO power supply < 1uA); When the pull-up resistor is externally connected, the 5V LDO still supplies power to the MCU after the LIN-PHY goes to sleep, and the MCU can go to sleep.

VCC is the pre-drive power supply integrated inside the chip. It is not affected during hibernation and can be powered down during hibernation.

VBAT independently powers the chip LIN-PHY and VIN powers the 5V LDO. Normally, there is no power loss during hibernation.

The LIN TXD pin has a 500kΩ pull-down resistor and the SLP _ N pin has a 500kΩ pull-down resistor.

21.1 Work mode

The LIN transceiver has four main modes of operation: sleep mode, standby mode, normal mode, and power-up mode.

Sleep mode: This is the lowest-power mode and can be woken up remotely via the LIN pin or directly via the SLP_N pin. To wake up in sleep mode, the remote wake-up time from the LIN pin must be greater than $t_{wake(dom)LIN}$ (150μs for LIN), and the direct wake-up time from the SLP_N pin must be greater than $t_{gotonorm}$ (10μs).After the LIN-PHY is woken up, the MCU core can be further woken up via the P1.1 pin.

Standby mode: When a local or remote wake-up event is detected while in sleep mode, the device automatically enters standby mode immediately, and a low level on the RXD pin indicates the wake-up process. The INH pin is set high when the part enters standby mode from sleep mode.

When the SLP_N pin is set high in standby mode, the following conditions may occur:

(1) Immediately reset the wake-up source flag; causes a possible strong pull-down state on the TXD to be released before the actual mode switch is performed (after $t_{gotonorm}$).

(2) When the high level on the SLP_N pin is maintained longer than $t_{gotonorm}$, the device enters normal mode.

(3) The wake-up request signal on the RXD pin is immediately reset.

Normal mode: LIN bus level is 12V. When LIN is received, it is converted to 5V and sent to MCU through RXD. When sending, MCU TXD is converted to 12V and output to the bus. In sleep, standby, or power-up mode, the device enters normal mode as long as the SLP_N pin is held high for longer than $t_{gotonorm}$. If the low level on the SLP_N pin is maintained longer than $t_{gotosleep}$ (10μs), the part switches to sleep mode.

Power-up mode: When in power-up mode, the RXD pin is floating and the TXD pin is weakly pulled down, but neither the transmitter nor the receiver is active. If the SLP_N pin is held high longer than $t_{gotonorm}$, the part enters normal mode.

In normal mode, the enters sleep mode when a falling edge occurs on the SLP_N pin and the SLP_N is held low longer than $t_{gotosleep}$. In sleep mode, the INH pin is always floating, and in other modes, the INH pin is high, and the 5V LDO enable EN can be controlled by an external pull-up or pull-down resistor. If it is externally pulled up, the 5V LDO will always maintain power supply, and if it is pulled down, the power supply to the MCU will be stopped during sleep, and the overall sleep power consumption of the chip will be lower. If INH is pulled down externally, it is not recommended to use the SLP_N to enter the sleep mode, because the MCU power supply will be turned off once the sleep mode is entered, resulting in the SLP_N floating out of control.

21.2 BSM Automatic addressing

Automatic addressing of the BSM (Bus shunt method), actuation of the tertiary current source and measurement of the voltage on the series resistance of the bus are performed within one bay field.

After receiving the address assignment command from the LIN master node, the MCU controls the opening or closing of the two current sources CS1 and CS2 through P1.1 and P1.2 of the MCU during the interval field of the next frame, and completes the voltage difference measurement on the series resistance of the LIN bus during the interval field. The built-in operational amplifier of MCU is used to amplify the voltage difference of the bus series resistance, and the amplified signal is sent to the ADC sampling port, and the sampling conversion is completed by the ADC inside the MCU.

For the first current measurement, CS1/2 is disconnected. At this time, only the pull-up resistor current of the traditional node flows through Rshunt. This current is called the background current and is recorded as I_{shunt1}.

For the second current measurement, CS1 is closed, the current flowing through the slave node R_{shunt} closer to the host is larger, at this time, the current flowing through R_{shunt} is recorded as I_{shunt2}, if I_{shunt2}-I_{shunt1} > I_{diff}, These nodes (denoted as $Node_{out\_of\_Pre\text{-}selection}$) are not considered to be the farthest. This process is called Pre-selection.

In the third current measurement, the current on one or a small number of slave nodes (denoted as $Node_{in\_of\_Pre\text{-}selection}$)$R_{shunt}$ is less than the threshold I_{diff}, and these nodes participate in the third current measurement. During the third current measurement, $Node_{out\_of\_Pre\text{-}selection}$ turns off CS1 and $Node_{in\_of\_Pre\text{-}selection}$ turns on CS1 and CS2. Because the number of $Node_{out\_of\_Pre\text{-}selections}$ is small, it does not result in excessive current sinking at the master node. The current flowing through R_{shunt} at this time is recorded as Ishunt3.If I_{shunt3}-I_{shunt1} > I_{diff}, these nodes (denoted as $Node_{out\_of\_Pre\text{-}selection}$) are not considered to be the farthest. If there is no traditional LIN node after the farthest node, the farthest node R_{shunt} has no current flowing through it, so it is identified as the farthest nodes and receives the slave address sent by the master node. This process is called Selection.

21.3 LIN-PHY Module parameters

Parameters	Min.	Typ.	Max.	Unit	Description
Limit parameters					
Supply voltage V_{BAT}	-0.3		+58.0	V	Relative to the ground
LIN Bus voltage V_{LIN}	-58.0		+58.0	V	Relative to the ground
INH Pin voltage V_{INH}	-0.3		V_{BAT}+0.3	V	
INH Pin output current $I_{O(INH)}$	-50		15	mA	
Junction temperature T_J	-40		150	℃	
Storage temperature T_{STG}	-55		150	℃	

Recommended operating conditions					
Supply voltage V_{BAT}	5.5		27	V	Relative to the ground
LIN Bus voltage V_{LIN}	0		27	V	
Logic pin voltage V_{LOGIC}	0		5.25	V	
Electrical parameters					
DC characteristic（Power source）					
V_{BAT} Pin output current I_{BAT}	3	10	20	uA	Sleep mode： $V_{LIN}=V_{BAT}$， $V_{WAKE\_N}=V_{BAT}$， $V_{TXD}=0V$， $V_{SLP\_N}=0V$， $V_{BAT}=12V$
V_{BAT} Pin output current I_{BAT}	150	300	1000	uA	Standby mode (recessive)： $V_{INH}=V_{BAT}$， $V_{LIN}=V_{BAT}$，$V_{WAKE\_N}=V_{BAT}$， $V_{TXD}=0V$， $V_{SLP\_N}=0V$
V_{BAT} Pin output current I_{BAT}	200	620	1200	uA	Standby mode (dominant)： $V_{BAT}=12V$， $V_{INH}=12V$， $V_{LIN}=0V$， $V_{WAKE\_N}=12V$， $V_{TXD}=0V$， $V_{SLP\_N}=0V$
V_{BAT} Pin output current I_{BAT}	200	320	1200	uA	Normal mode (recessive)： $V_{INH}=V_{BAT}$， $V_{LIN}=V_{BAT}$，$V_{WAKE\_N}=V_{BAT}$， $V_{TXD}=5V$， $V_{SLP\_N}=5V$
V_{BAT} Pin output current I_{BAT}	0.6	1.3	2	uA	Normal mode (dominant)： $V_{BAT}=12V$， $V_{INH}=12V$，$V_{WAKE\_N}=12V$， $V_{TXD}=0V$， $V_{SLP\_N}=5V$
Power-on reset					
Low power-on-reset threshold voltage $V_{th(POR)L}$	1.6	3.3	3.9	V	
High power-on reset threshold voltage $V_{th(POR)H}$	2.3	3.6	4.3	V	
Power-on reset hysteresis voltage $V_{hys(POR)}$	0.05	0.3	1	V	
V_{BAT} Low level threshold voltage $V_{th(VBATL)L}$	3.9	4.3	4.7	V	
V_{BAT} High level threshold voltage $V_{th(VBATH)H}$	4.2	4.5	4.9	V	
V_{BAT} Hysteresis voltage $V_{hy(VBATL)}$	0.05	0.3	1	V	
INH Pin					
Turn on resistor R_{SW} from V_{BAT} to I_{NH}		20	50	Ω	In standby, normal, and power-on model： I_{INH}=-15mA;$V_{BAT}=12V$
High level leakage current I_{LH}	-5	0	5	uA	Sleep mode：

					V_{INH}=27V;V_{BAT}=27V
LIN Pin					
Driver dominant state limit current I_{BUS_LIM}	40		100	mA	V_{TXD}=0V;V_{LIN}=V_{BAT}=18V
Pull-up resistor R_{PU}	50	160	250	kΩ	Sleep mode： V_{SLP_N}=0V
Receiver recessive input leakage current $I_{BUS\_PAS\_rec}$			20	uA	V_{TXD}=5V;V_{LIN}= 27V;V_{BAT}=5.5V
Receiver dominant input leakage current $I_{BUS\_PAS\_dom}$	-600			uA	Normal mode;V_{TXD}=5V;$_{VLIN}$= 0V;V_{BAT}=12V
Voltage drop of series diode $V_{SerDiode}$	0.4	0.7	1	V	Pull path on R_{slave}， $I_{SerDiode}$=10μA
Bus current without ground $I_{BUS\_NO\_GND}$	-750		10	uA	V_{BAT}=27V; V_{LIN}= 0V
Bus current without power $I_{BUS\_NO\_BAT}$			10	uA	V_{BAT}=0V; V_{LIN}= 27V
Receiver dominant flip threshold voltage V_{BUSdom}			0.4V_{BAT}	V	
Receiver recessive flip threshold voltage V_{BUSrec}	0.6V_{BAT}			V	
Receiver center-flip threshold voltage V_{BUS_CNT}	0.475		0.525	V_{SUP}	V_{BUS_CNT}=(V_{th_dom}+ V_{th_rec})/2[e]
Receiver hysteresis threshold voltage V_{HYS}			0.175 V_{BAT}	V	V_{HYS}=V_{BUSrec} -V_{BUSdom}
From the electrical resistance R_{slave}	20	30	47	kΩ	Resistance between LIN and V_{BAT}, V_{LIN}=0V;V_{BAT}=12V
LIN Pin equivalent capacitance C_{LIN}			30	pF	
Dominant output voltage $V_{O(DOM)}$			1.4	V	Normal mode; V_{TXD}=0V;V_{BAT}= 7V
			2.0	V	Normal mode; V_{TXD}=0V;V_{BAT}= 18V
Thermal shutdown					
Shutdown junction temperature $T_{jsd(sd)}$	160	175	200	℃	
Hysteresis temperature $T_{jsd(hys)}$		20		℃	
Duty cycle					
δ1[1][2] Duty cycle 1	0.396				$V_{th(rec)(max)}$=0.744xV_{BAT}; $V_{th(dom)(max)}$=0.581xV_{BAT}; t_{bit}=50μs; V_{BAT}=7~18V
	0.396				$V_{th(rec)(max)}$=0.76xV_{BAT}; $V_{th(dom)(max)}$=0.593xV_{BAT};

					t_{bit}=50μs; V_{BAT}=5.5~7V
δ2[2][3] Duty cycle 2			0.581		$V_{th(rec)(min)}$=0.422xV_{BAT}; $V_{th(dom)(min)}$=0.284xV_{BAT}; t_{bit}=50μs;V_{BAT}=7.6~18V
			0.581		$V_{th(rec)(min)}$=0.41xV_{BAT}; $V_{th(dom)(min)}$=0.275xV_{BAT}; t_{bit}=50μs;V_{BAT}=6.1~7.6V
δ3[1][2] Duty cycle 3	0.417				$V_{th(rec)(max)}$=0.778xV_{BAT}; $V_{th(dom)(max)}$=0.616xV_{BAT}; t_{bit}=96μs; V_{BAT}=7~18V
	0.417				$V_{th(rec)(max)}$=0.797xV_{BAT}; $V_{th(dom)(max)}$=0.630xV_{BAT}; t_{bit}=96μs;V_{BAT}=5.5~7V
δ4[2][3] Duty cycle 4			0.590		$V_{th(rec)(min)}$=0.389xV_{BAT}; $V_{th(dom)(min)}$=0.251xV_{BAT}; t_{bit}=96μs;V_{BAT}=7.6~18V
			0.590		$V_{th(rec)(min)}$=0.378xV_{BAT}; $V_{th(dom)(min)}$=0.242xV_{BAT}; t_{bit}=96μs;V_{BAT}=6.1~7.6V
Timing characteristics					
Bus fall timet_f[2]			22.5	μs	
Bus rise timet_r[2]			22.5	μs	
Bus Rise and Fall Time $\Delta t_{(r-f)}$[2]	-5		5	μs	
Transmitter propagation delay $t_{P(TX)}$[2]			6	μs	
Transmitter propagation delay symmetry $t_{P(TX)sym}$[2]	-2.5		2.5	μs	
Receiver propagation delay $t_{P(RX)}$[4]			6	μs	
Receiver propagation delay symmetry $t_{P(RX)sym}$[4]	-2		2	μs	
LIN Explicit Wakeup Time (Remote Wakeup) $t_{wake(dom)LIN}$	30	80	150	μs	
WAKE_N Explicit Wake-up Time (BenTo wake up) $t_{wake(dom)WAKE\_N}$	7	30	50	μs	
Time to enter normal mode $t_{gotonorm}$	2	5	10	μs	
Time to enter sleep mode $t_{gotosleep}$	2	5	10	μs	
TXD Explicit timeout $t_{to(dom)TXD}$	27	55	90	ms	

[1] δ1, δ3=$t_{bus(rec)(min)}/2\times t_{bit}$

[2] Bus load condition：(1)C_{BUS}=1nF,R_{BUS}=1kΩ；(2) C_{BUS}=6.8nF,R_{BUS}=660Ω；(3) C_{BUS}=10nF,R_{BUS}=500 Ω

[3] δ2, δ4=$t_{bus(rec)(max)}/2\times t_{bit}$

[4] Receiver Output Pin RXD Load Condition： C_{RXD}=20pF,R_{RXD}=2.4kΩ

22 General Purpose Peripherals

- One UART works in the full-duplex operation mode, supporting 8/9 bits of data, 1/2 stop bit(s), odd/even/no parity mode, with 1 byte send cache, 1 byte receive cache, with Multi-drop Slave/Master mode, and the baud rate ranging from 300-115200
- One SPI for master-slave mode
- One IIC for master-slave mode
- Hardware watchdog, driven by RC timer, being independent of system high speed timer, write-in protection

23 Special IO Multiplexing

Precautions for LKS03x special IO multiplexing

The SWD protocol consists of two signal lines: SWCLK and SWDIO. The former is a timer signal that, for the chip, is the input state and does not change the input state. The latter is a data signal that switches between an input state and an output state during data transmission for the chip, which defaults to the input state.

LKS32AT037PXL5M6Q9 can realize the function of multiplexing two IOs of SWD into other IOs. IO multiplexed by SWCLK is P1.8, and IO multiplexed by SWDIO is P1.9. The precautions are as follows:

- ➢ Multiplexing is disabled by default, and software is needed to write a 0 to SYS_IO_CFG [6] to enable the multiplexing. That is, after the hard reset of the chip is complete, the initial state is for SWD. The two IOs of the SWD have a pull-up inside the chip (the pull-up resistance of the chip is about 10K). When IO functions as SWD, the pull-up is turned on by default and cannot be turned off. When IO functions as GPIO, pull-up can be worked via GPIO1_PUE [8] and GPIO1_PUE [9]. P1.8 and P1.9 are fixed as SWD functions within 30ms of chip power-on reset, the software can write 0 to SYS_IO_CFG [6], but IO function switching takes effect after 30ms. LRC counting was used for 30ms with some deviation due to process reasons.
- ➢ When multiplexing is enabled, tools such as KEIL cannot directly access the chip, that is, Debug and erase download are unavailable. There are two options if you need to re-download the program.
- ● Firstly, it is recommended to use Linko dedicated offline downloader to erase. It is recommended to reserve a certain margin for the time for enabling software multiplexing, for example, approximately 100ms, to ensure that the offline downloader can be erased to prevent deadlock. The amount of margin is to ensure the success rate of offline downloader erasure. The larger the margin, the greater the probability of a successful one-time erase.
- ● Secondly, there is an exit mechanism inside the program. For example, the change of some other IO level (generally as input) indicates that the external needs to use SWDIO in software reconfiguration and de-multiplexing. At this point, the KEIL function can be restored.

In the packaging of SSOP24, QFN40, and SOP16L, SWDIO, SWCLK may have bonded with other IOs. At this point, it should be noted that other IO action may cause the chip to misinterpret the SWD action.

The considerations for SWCLK multiplexing are as follows:

- ➢ Multiplexing is disabled by default, and software is needed to enable the multiplexing. That is, after the hard reset of the chip, the initial state is used for SWCLK, which is pulled up inside the chip (the internal pull-up resistance of the chip is about 10K). Please pay attention if the initial level is required by the application.
- ➢ When multiplexing is enabled, tools such as KEIL cannot directly access the chip, that is, Debug and erase download are unavailable. There are two options if you need to re-download the program.

- Firstly, it is recommended to use Linko dedicated offline downloader to erase. It is recommended to reserve a certain margin for the time for enabling software multiplexing, for example, approximately 100ms, to ensure that the offline downloader can be erased to prevent deadlock. The amount of margin is to ensure the success rate of offline downloader erasure. The larger the margin, the greater the probability of a successful one-time erase.
- Second, there is an exit mechanism inside the program. For example, the change of some other IO level (generally as input) indicates that the external needs to use SWCLK in software reconfiguration and de-multiplexing. At this point, the KEIL function can be restored.

If only SWCLK is multiplexed and SWDIO is not multiplexed at this point, please refer to the above precautions.

RSTN signal is used for external reset pins for the LKS32AT037PXL5M6Q9 chip by default.

LKS32AT037PXL5M6Q9 can realize the functions of RSTN multiplexing into other IO. The multiplexed IO is P0.2. The precautions are as follows:

- Multiplexing is disabled by default, and software is needed to write a 1 to SYS_IO_CFG [5] to multiplex RSTN as a normal GPIO. That is, the initial state of the chip is used for RSTN, which is pulled up inside the chip (the internal pull-up resistance of the chip is about 100K). Please pay attention if the initial level is required by the application.
- The default state is RSTN. Program execution can only be started after RSTN is released normally. The application needs to ensure that RSTN has adequate protection, such as peripheral circuit pull-up. If capacitance can be added, it is better.
- When multiplexing is enabled, the RSTN function becomes invalid. If a hard reset of the chip is required, the source can only be powered down/watchdog.
- RSTN multiplexing does not affect the use of KEIL.

24 Ordering Information

Device	Package Size	Quantity per disc/tube	Quantity in box	Quantity in case
LKS32AT037PXL5M6Q9	QFN24	490/disc	4900PCS	29400PCS

25 Version History

Table 25-1 Document Version History

Time	Version No.	Description
05/13/2025	1.6	Pin Function Selection modified
04/30/2025	1.32	Adding the description that the chip can support driving a BLDC motor with a phase current RMS value of 1A when the maximum ring temperature of the chip is 105 degrees.
04/16/2025	1.31	Delete the description of GPIO quantity.
03/17/2025	1.30	Add AT037PXL5M6Q9 EN datasheet.

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For earlier versions, please refer to this document.